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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,575	06/06/2005	Adrianus Willem Ludikhuize	NL02 1358 US	6697
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NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131				
EXAMINER				
HU, SHOUXIANG				
ART UNIT		PAPER NUMBER		
2811				
NOTIFICATION DATE		DELIVERY MODE		
03/10/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/537,575

Applicant(s)

LUDIKHUIZE ET AL.

Examiner

Shouxiang Hu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2008.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
4a) Of the above claim(s) 4-7 and 12 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3 and 8-11 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date 6/6/2005; 5/30/06
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species 1 in the reply filed on January 09, 2008 is acknowledged. The traversal is on the ground(s) that all claims share the same technical features recited in claim 1 and/or that the species have not been properly identified as being mutually exclusive. This is not found persuasive because:

The species as identified in the previous office action are independent or distinct because of the patentably distinctive characteristics readily apparent in the corresponding figures identified above. For example, the feature of the vertical DMOS FET (VDMOS) which is recited in claims 2 and/or 3, as the VDMOS 202 shown in Species 1 of the embodiment of Fig. 2a, is obviously unreadable on what is shown in the Species 3 of the embodiment of Fig. 3, wherein the SF 302 is formed of a LDMOS (as what is recited in claims 4 and/or 12). These species are obviously mutually exclusive, since the recited SF cannot be formed of and/or include both of the LDMOS and VDMOS at the same time. And, they are mutually distinctive because of the substantially distinctive structures between the LDMOS and the VDMOS. Accordingly, these species lack the same technical feature of a substantially similar type SF in the claimed inventions, regardless whether they may each be readable on the broader invention defined in claim 1.

Furthermore, no full support can be found in the original disclosure for the subject matters that the SF can include both the LDMOS and the VDMOS at the same time, and/or that the feature of the multiple conductive plugs as recited in claims 5-7 (as

shown in embodiment of Fig. 2b, i.e., Species 2) could also be applicable to the embodiment of Fig. 2a.

Although only a few of classes/subclasses were given in the 08-20-2007 office action, they are only the exemplary ones. Because the subject matters recited in the claims are strongly circuitry-oriented, which are far beyond the normal coverage of Class 257. Along with required key word search, a thorough search would be required in each of the classes/subclasses: 257/327-346, 618+ and 773+; 323/224+ and 383+; 363/15+; 361/84+; and 327/543+, if all species have to be examined. Thus, search and examination of all of the claims with all the species would impose a substantially undue burden upon the examiner.

Therefore, the requirement of election among the identified species is still deemed proper. Thus, claims 4-7 and 12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being unreadable on the elected Species 1, while claims 1-3 and 8-11 remain active in this office action.

Nevertheless, applicant is reassured that, upon the allowance of any of the active claims (claims 1-3 and 8-11), applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of the allowed claim(s).

Claim Objections

2. Claims 8 and 9 are objected to because of the following informalities and/or defects:

In claims 8 and 9, the term of "polarity" should read as: --polarities--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8 and 9, insofar as being supported by the elected species, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 and 9 each recite the subject matter that the vertical DMOS FET and LDMOS FET are formed in respective wells having opposite polarity. However, it is not clear whether it means that the entire vertical DMOS FET or only a portion of it is formed in one of the two wells, given that at least the drain region (204)—an integral part of the vertical DMOS FET (202) is not formed inside any well in the elected species of the embodiment of Fig. 2a.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 8, 10 and 11, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Sumida (US 5,818,282).

Sumida discloses a power/voltage converter, including an integrated circuit (a half-bridge circuit; see Figs. 2 and 4; also see col. 6, lines 28-34), comprising a CF (Q22, a LDMOS FET); and a SF (Q21; a VDOS FET), wherein the CF and the substrate (23) are both n type; and the Q22 and Q21 can naturally respectively function as a CF and an SF therein, because the two FETs in a half-bridge circuit such as that (Q1 and Q2) shown Fig. 2 of Sumida is symmetrical, and any one of the two the FETs can naturally contribute to the control of the power/voltage output of the converter, while the other of the two FETs is always inherently required to operate in a synchronous manner in such a half-bridge circuit.

Furthermore, it is noted that the recitation of the term "down" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 8, it is further noted that, insofar as being in compliance with 35 U.S.C. 112, in Sumida the vertical DMOS FET has an n-type well (25a and/or 25) and the LDMOSFET has a p-type well (27 and/or 27a).

Regarding claim 10, it is further noted that the SF and CF in Sumida does not include any insulative isolation regions therebetween.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 9, insofar as being compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sumida in view of Hshieh'367 (Hshieh et al., US 2001/0003367) and/or Hshieh'788 (Hshieh et al., US 2001/0008788).

The disclosure of Sumida is discussed as applied to claims 1, 2, 8, 10 and 11 above.

Although Sumida does not expressly disclose that the vertical DMOS FET can be formed of trench-type, one of ordinary skill in the art would readily recognize that the trench-type vertical DMOS FET can be desirably formed so as to reduce the device size, and/or to increase the speed, and/or to lower the specific on-resistance, as readily evidenced in Hshieh'367 (see [0014]—[0016]), and/or in Hshieh'788 (see [0004]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the art-known vertical trench DMOS FET, such as the one of Hshieh'367 and/or in Hshieh'788, into the device of Sumida, so that

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an integrated circuit device with reduced size and/or with improved performance would be obtained.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-I are cited as being related to a half-bridge circuit structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
Primary Examiner, Art Unit 2811
February 27, 2008